REMARKS

Claims 1-16 are all the claims that are pending in the application.

Applicant has amended claims 1, 4, 9 and 11-16. The amendments are not made for reasons of patentability and are not intended to narrow the scope of the claims, and thus are not subject to estoppel.

Applicant thanks the Examiner for stating that claims 3 and 7 would be allowable if rewritten to independent form including all the limitations of the base claim and intervening claims. However, because Applicant believes that the independent claims should be allowable for at least the reasons discussed below, Applicant is not rewriting these claims at this time.

Applicant thanks the Examiner for acknowledging the claim for foreign priority under 35 U.S.C. § 119, and receipt of a certified copy. Additionally, Applicant thanks the Examiner for indicating the drawings filed on December 10, 2003, are accepted.

Also, the Applicant thanks the Examiner for considering the references cited in IDS filed on January 12, 2006 and December 12, 2005.

Claim Objections

Claim 16 has been amended to include the period at the end of the claim. Thus, withdrawal of this objection is respectfully requested.

Claim Rejections - 35 U.S.C. § 112 Second Paragraph

Claims 1 and 6 are amended to include the proper antecedent basis as the Examiner requested. Therefore, claims 1-8 should now be allowed under 35 U.S.C. § 112. Therefore, Applicant respectfully requests that the rejection of claims 1-8 be withdrawn.

Claim Rejections - 35 U.S.C. § 102

Claims 11 and 14 have been rejected under 35 U.S.C. § 102(e) as being anticipated by Shimizu (6,894,982). Applicant traverses these rejections because Shimizu fails to disclose or suggest all of the claim limitations. Specifically, Shimizu fails to disclose or suggest at least the following:

Claim 11:

delaying said interrupt signal for operating said CPU during a time interval when said receiving frame signal is active;

applying said interrupt signal to the CPU after said receiving frame signal is inactivated; and

operating said CPU in response to said interrupt signal.

Claim 14:

delaying an interrupt signal for operating said CPU during a time interval when said receiving frame signal is active;

applying said interrupt signal to the CPU after said receiving frame signal is inactivated; and

operating said CPU in response to said interrupt signal.

The Examiner alleges that Shimizu figure 1, and column 2 line 61 to column 3 line 5, column 3 lines 20-40, column 3 lines 36-40, and column 4 lines 17-46 disclose or suggest all of the limitations of claims 11 and 14. Applicant respectfully disagrees.

Shimizu does not disclose the claim limitation of delaying an interrupt signal for operating the CPU during a time interval when said receiving frame signal is active. Shimizu provides two separate interrupt signals (b) and (c), "both a start interrupt signal (b) which is synchronized with a starting timing of this TCH frame signal (a) and an end interrupt signal (c) which is synchronized with and end timing for the TCH frame signal (a) . . ." (col. 3 lines 31-35). These interrupt signals in Shimizu are not delayed and do not apply to the operation of the CPU.

Additionally, the Examiner cites column 3 lines 20-40, column 3 lines 36-40, and column 4 lines 17-46 that the interrupt signal controls the CPU. However, column 3 lines 20-40 discloses that "the CPU starts controlling an operational clock frequency in response to this start interrupt signal . . ."(col. 3 lines 36-37). Shimizu discloses that this response to the start interrupt signal will control the clock frequency for the CPU and does not disclose the claimed limitation for operating the CPU in response to the interrupt signal (also see figure 6).

Therefore, Applicant respectfully submits that independent claims 11 and 14 are patentable over the applied references.

Further, Applicants respectfully submit that rejected independent claims 12, 13, 15, and 16, are allowable, at least because of their dependency.

Claim Rejections - 35 U.S.C. § 103

Claims 12 and 15 have been rejected under 35 U.S.C. § 103(a) as being unpatentable over Shimizu in view of Turney (5,949,812). Applicant respectfully traverses these rejections because Turney fails to disclose or suggest all of the claim limitations. Specifically, the references fail to disclose or suggest at least the following limitations:

Claim 12:

stopping operation of said CPU when said receiving frame signal is activated; and

restarting operation of said CPU after said receiving frame signal is inactivated.

First, claim 12 should be allowable for the reasons discussed above in connection with claim 11, because Turney does not make up for the deficiencies of Shimizu noted above.

Next, the Examiner concedes that Shimizu fails to disclose the stopping and restarting operation of the CPU as claimed. In order to make up for the deficiency, the Examiner cites to Turney for allegedly disclosing the stopping and starting the CPU in order to save battery life.

Turney discloses stopping the CPU during idle times where the system clock generator is less than full speed in order to save battery life. (col. 4, line 22-42) Idle time indicates the receiving frame is inactive. However, Turney does not disclose the claim limitation of stopping the operation of the CPU when the receiving frame signal is activated. Turney discloses stopping the CPU during an idle time, which means the receiving frame is not active.

Therefore, because Turney fails to compensate for the above noted deficiency of Shimizu with regards to claim 12, the Examiner is requested to withdraw the prior art rejections.

With respect to claim 15, specifically, the references fail to disclose or suggest at least the following limitations:

Claim 15:

stops operation of said CPU when said receiving frame signal is activated; and

restarting operation of said CPU after said receiving frame signal is inactivated.

First, claim 15 should be allowable for the reasons discussed above in connection with claim 14, because Turney does not make up for the deficiencies of Shimizu noted above.

The Examiner concedes that Shimizu fails to disclose stopping and restarting operation of the CPU as claimed. In order to make up for the deficiency, the Examiner cites to Turney as disclosing stopping and starting of the CPU in order to save battery life.

As mentioned above with respect to claim 12, Turney fails to compensate for the above noted deficiency of Shimizu. Therefore, the Examiner is requested to withdraw the prior art rejections.

Claims 1-2, 8, 11-16 have been rejected under 35 U.S.C. § 103(a) as being unpatentable over Kobayashi (US 2001/0053703) in view of Yoshimoto (US 2002/0104890). Applicant respectfully traverses this rejection because the references fail to disclose or suggest all of the claim limitations. Specifically, the references fail to disclose or suggest at least the following limitations:

Claims 1:

said radio circuit block receiving a radio signal through said antenna during a receiving slot, wherein said control block stops operation of said CPU during said receiving slot.

With respect to Claim 1, the Examiner concedes that Kobayashi fails to disclose that the control block stops operation of a CPU during a receiving slot. (OA page 5) In order to make up this deficiency, the Examiner cites to Yoshimoto as disclosing stopping of a CPU when a communication device is in a receiving mode in order to reduce noise generated from the CPU. The Examiner also alleges that one skilled in the art would have combined the Yoshimoto stop operation with Kobayashi in order to reduce noise generated from the CPU during the receiving slot. Applicant respectfully disagrees.

Yoshimoto does not disclose the claim limitation that stops operation of the CPU when the receiving frame signal is activated. Yoshimoto relates to IC cards that are used in the railway systems and public phones that are capable of suppressing the influence of noise caused by the operation of a nonvolatile memory (page 1 par. [0002] and [0005]). However, Yoshimoto does not mention that these IC cards can be used in cell phones or in other devices that uses radio signals. Also, Yoshimoto does not discuss IC cards for an operation related to a radio circuit block receiving a radio signal through the antenna during a receiving slot, wherein the control block stops operation of the CPU during the receiving slot. The claimed receiving slot relates to the time during which a radio signal is received. Yoshimoto discloses, "the CPU can be prevented form being kept in the halt state, for example, when a receive data cannot be received for a long period of time after the data transmission circuit **102** going in the receive state" (page 9 par. [0191]) Therefore, Yoshimoto does not discloses the claimed limitation that stops operation of the CPU during the receiving slot.

Therefore, because Yoshimoto fails to compensate for the above noted deficiency of Kobayashi with regards to claim 1, Applicant respectfully submits that independent claim 1 is patentable over the applied references.

Regarding claims 2, 4-6, and 8, they should be allowable at least based on their dependency from claim 1 for the same reasons.

As to claim 11, Yoshimoto fails to disclose at least the following limitations:

delaying said interrupt signal for operating said CPU during a time interval when said receiving frame signal is active;

applying said interrupt signal to the CPU after said receiving frame signal is inactivated;

Yoshimoto does not disclose the claim limitation delaying the interrupt signal for operating the CPU during a time interval when the receiving frame signal is active. As discussed above in connection with claim 1, Yoshimoto does not discuss the use of IC cards for an operation related to a radio circuit block receiving a radio signal through said antenna during a

receiving slot. Additionally, Yoshimoto does not disclose the claim limitation for apply this interrupt signal to the CPU after the receiving frame is inactive.

Therefore, Applicant requests that the Examiner withdraw the rejection of claim 11.

Additionally, claims 12 and 13 should be allowable at least by virtue of their dependency.

As to claim 14, as discussed in connection with claims 1 and 11 above, Yoshimoto fails to disclose the following limitations:

delaying an interrupt signal for operating said CPU during a time interval when said receiving frame signal is active;

applying said interrupt signal to the CPU after said receiving frame signal is inactivated;

Therefore, Applicant respectfully submits that claim 14 is allowable and requests that the Examiner withdraw the rejection of claim 14.

Additionally, claims 15 and 16 should be allowable at least by virtue of their dependency.

Claims 9 and 10 have been rejected under 35 U.S.C. § 103(a) as being unpatentable over Kobayashi in view of Miyake (6,222,985). Applicant respectfully traverses this rejection because the references fail to disclose or suggest all of the claim limitations. Specifically, the references fail to disclose or suggest at least the following highlighted limitations:

Claim 9:

at least one of display block and camera block, and a control block for controlling operation of said blocks, said control block including a central processing unit (CPU), **said radio circuit block receiving a radio signal through said antenna during a receiving slot**, wherein said at least one of display block and camera block **stops data transmission through an associated bus during said receiving slot.**

The Examiner concedes that Kobayashi fails to disclose that; at least one of display block and camera block stops data transfer through an associated bus during a receiving slot (OA page 7). To remedy this deficiency, the Examiner applies Miyake, alleging that it discloses or

suggests that one skilled in the art would have combined the teaching of Miyake to Kobayashi, in order to reduce noise generated from the display block and camera block during the receiving slot (OA page 7). Applicant respectfully disagrees.

Miyake does not disclose the claimed receiving slot. Miyake discloses a camera which records positional data, which is obtained by a GPS unit during photographing, and image on a memory card. However, Miyake does not disclose a radio circuit block receiving a radio signal through an antenna during a receiving slot, wherein at least one of display block and camera block stops data transmission through an associated bus during the receiving slot. Specifically, Miyake does not disclose a radio signal, receiving slot, or that data is stopped through any bus. The Examiner argues that Miyake discloses "when receiving data from the GPS unit **160** the main CPU **100** stops the DC/DC **52** converter of the image pickup unit **40** to thereby stop supplying the clock generating **46** circuit with electricity" (col. 8 lines 61-64 and figure 1) as possibly being the data bus being stopped. However, this does not disclose a data bus. Therefore, Miyake does not disclose the claim limitation of receiving a radio signal through the antenna during a receiving slot or that data is stopped through a bus.

Therefore, Applicant respectfully submits that claim 9 is allowable and requests that the Examiner withdraw the rejection of claim 9. Also, Applicant submits that claim 10 is allowable, at least because of its dependency.

Conclusion

In view of the above, reconsideration and allowance of this application are now believed to be in order, and such actions are hereby solicited. If any points remain in issue which the Examiner feels may be best resolved through a personal or telephone interview, the Examiner is kindly requested to contact the undersigned at the telephone number listed below.

The USPTO is directed and authorized to charge all required fees, except for the Issue Fee and the Publication Fee, to Deposit Account No. 19-4880. Please also credit any overpayments to said Deposit Account.

Respectfully submitted,

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